VLSI for DSP

Homework No.2 79882304 黃郁書

Design 3x3 systolic matrix multiplication by logic gates.

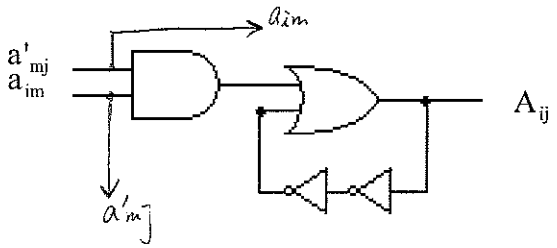
A-

Ans.

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} \begin{bmatrix} a'_{11} & a'_{12} & a'_{13} \\ a'_{21} & a'_{22} & a'_{23} \\ a'_{31} & a'_{32} & a'_{33} \end{bmatrix} = \begin{bmatrix} A_{11} & A_{12} & A_{13} \\ A_{21} & A_{22} & A_{23} \\ A_{31} & A_{32} & A_{33} \end{bmatrix}$$

$$A_{11} = a_{11}a'_{11}+a_{12}a'_{21}+a_{13}a'_{31}$$
$$A_{12} = a_{11}a'_{12}+a_{12}a'_{22}+a_{13}a'_{32}$$
$$A_{13} = a_{11}a'_{13}+a_{12}a'_{23}+a_{13}a'_{33}$$
$$A_{21} = a_{21}a'_{11}+a_{22}a'_{21}+a_{23}a'_{31}$$
$$A_{22} = a_{21}a'_{12}+a_{22}a'_{22}+a_{23}a'_{32}$$
$$A_{23} = a_{21}a'_{13}+a_{22}a'_{23}+a_{23}a'_{33}$$
$$A_{31} = a_{31}a'_{11}+a_{32}a'_{21}+a_{33}a'_{31}$$
$$A_{32} = a_{31}a'_{12}+a_{32}a'_{22}+a_{33}a'_{32}$$
$$A_{33} = a_{31}a'_{13}+a_{32}a'_{23}+a_{33}a'_{33}$$

So $A_{ij} = \sum_{m=1}^{3} a_{im}a'_{mj}$



VLSI for DSP

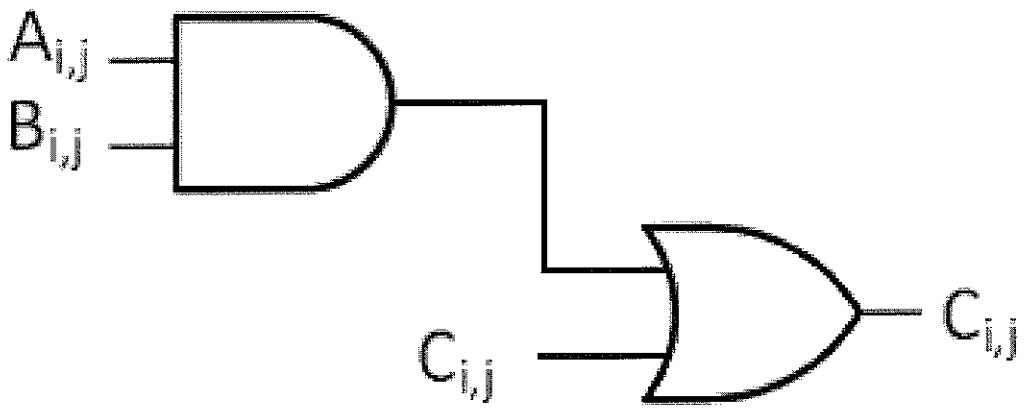
Homework 2

資工碩一 79883107 蔡維峻

B

(a) Design 3x3 systolic matrix multiplication by logic gates.

Ans:



VLSI for DSP

1978101

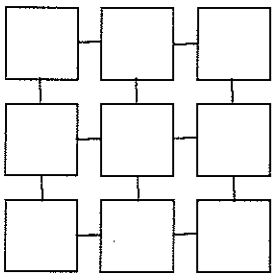
Homework No.2

陳弘喬

You can choose one of them or answers all the questions.

(a) Design 3x3 systolic matrix multiplication by logic gates.

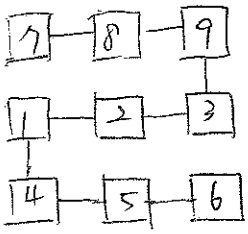
(b) There are 9 processors connected each other like figure 1. Place 1 to 9 numbers in the processor Randomly. Try to sort numbers in the processor array.



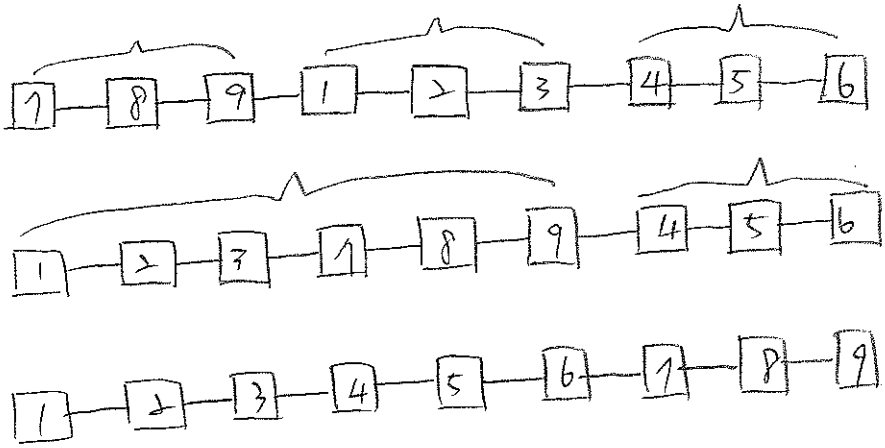
B-

(c) How to sorting the numbers in time O(1). Hint: 3D mesh.

(b)

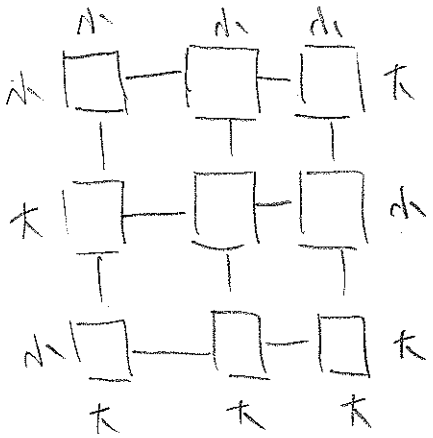


Bubble sort



Homework 2

(B)



swap(c1, c2)

swap(c2, c3)

swap(c1, c3)

swap(r1, r2)

swap(r2, r3)

swap(r1, r3)

repeat