國立臺北大學電機工程研究所教師研究成果清單

期刊論文

陳永源教授
詹景裕教授
黃弘一副教授
劉萬榮教授
林嘉洚教授
楊棧雲教授

研討會議論文

陳永源老師
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專書、技術報告

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專利

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【SCI/SCIE/SSCI/EI 總計表】

教師姓名	SCI	SCIE	SSCI	EI	其他	總計
陳永源教授	18	4	0	22	0	44
劉萬榮教授	12	1	0	1	0	14
詹景裕教授	10	0	0	3	0	13
何善輝教授	4	3	0	0	2	9
林嘉洚教授	21	3	0	3	0	27
楊棧雲教授	10	0	0	4	0	14
黃弘一副教授	0	0	0	0	8	8
總計	**75**	**11**	**0**	**33**	**10**	**129**

【期刊論文】

詹景裕教授

1. V. Shen and Gene Eu Jan, "Machine Learning Petri Nets," to appear in *IEEE Transactions on Systems, Man, and Cybernetics- Part A: Systems and Humans*, 2009. (Regular paper, SCI)

2. Chien-Long Shih, Chien-Min Su, Gene Eu Jan, and Bin Lin, "Efficient Route Planning for ECDIS with Current," to appear in *Navigation Quarterly*, 2009.

3. Gene Eu Jan, Ki-Yin Chang, and Ian Parberry, 〝Optimal Path Planning for Mobile Robot Navigation,〞 *IEEE/ASME Transaction on Mechatronics,* Vol. 14, No. 9, pp. 925- 936, Aug. 2008. (Regular paper, SCI)

4. Ki-Yin Chang, Gene Eu Jan, C. M. Su and Ian Parberry, 〝Optimal Interceptions on Two-Dimensional Grids with Obstacles," *Journal of Navigation*, Vol. 61, pp. 31~43, Jan. 2008. (SCI)

5. Wan-Rone Liou, Tsung-Hsing Chen, Mei-Ling Yeh, Jyh-Jier Ho and Gene Eu Jan, 〝A Low-Power 2/5.8-GHz Dual-Wide-Band CMOS LC-VCO with Switched- Inductor Technique,〞 *International Journal of Electronics,* Vol. 94, No. 6, pp. 623~632, June 2007. (SCI)

6. Gene Eu Jan, P. S. Hong, C. M. Su and F.-Y. Lin, 〝Optimal Path Problem for Aircraft in Quadric Surface," *Journal of Aeronautics, Astronautics and Aviation*, Vol. 39, No. 2, pp. 197~202, Oct. 2007. (EI)

7. Ming-Bo Lin, Jang-Feng Lee, and Gene Eu Jan, 〝A Lossless Data Compression and Decompression Algorithm and Its Hardware Architecture,〞 *IEEE Transactions on VLSI Systems*, Vol. 14, No. 9, pp. 925-936, Sept. 2006. (Regular paper, SCI)

8. Gene Eu Jan and Shao-Wei Leu, Cheng-Hong Li and Xiaoshe Dong, 〝Perfect Load Balancing on Cube-Connected Cycles Multiprocessors,〞 *WSEAS Trans. on Computers Research*, Issue 1, Vol. 1, pp. 13~ 18, Nov. 2006. (EI)

9. Ki-Yin Chang, Gene Eu Jan, Lsword Lou and Zhi-Ping Yin, "The Optimal Path-Planning for Mobile Vehicles with GPS on 3-D Electronic Maps," *Journal of Aeronautics, Astronautics and Aviation*, Vol. 38, No. 1, pp. 63~70, 2006. (EI)

10. Gene Eu Jan, Ki-Yin Chang, Su Gao and Ian Parberry, 〝A 4-Geometry Maze Router and Its Application on Multi-terminal Nets,〞 *ACM Transactions on Design Automation of Electronic Systems*, Vol. 10, No. 1, pp. 116-135, Jan. 2005. (SCI)

11. Gene Eu Jan and Ming-Bo Lin, 〝Concentration, Load Balancing, Partial

Permutation Routing and Superconcentration on Cube- Connected Cycles Parallel Computers,〞 *Journal of Parallel and Distributed Computing,*, No. 65, pp. 1471~ 1482, Dec. 2005. (Regular paper, SCI)

12. Gene Eu Jan and Yuan-Shin Huang, 〝Hierarchical Interconnection Networks Based on (3,3)-Graphs for Massively Parallel Processors,〞 *IEICE Trans. on Information and Systems*, Vol. E87-D, No. 7, pp. 1649~1656, July 2004. (SCI)

13. Wan-Rone Liou, Chun-An Tsai, Mei-Ling Yeh, and Gene Eu Jan, 〝A 5.2 GHz Low-voltage Low Noise Amplifier with 0.35 um CMOS Technology,〞 *International Journal of Electronics*, pp. 551~561, Sep. 2004. (SCI)

14. Gene Eu Jan, Yuan-Shin Huang, Ming-Bo Lin, and Deron Liang, 〝Novel Hierarchical Interconnection Networks for High- Performance Multicomputer Systems,〞 *Journal of Information Science and Engineering*, Vol. 20, No. 6, pp. 1213~1229, Nov. 2004. (SCI)

15. Gene Eu Jan, S. W. Leu and Cheng-Hung Li, 〝On the Array Embeddings and Layout of Quadtrees and Pyramids,〞 *Journal of Information Science and Engineering*, Vol. 20, No. 1, pp. 127~141, Jan. 2004. (SCI)

黃弘一副教授

International Journal Papers

1. Hong-Yi Huang and Ruei-Iun Pu “Current-Mode Bidirectional Transceiver with Impedance Matching” revised by Microelectronics, Journal.
2. Hong-Yi Huang, Wei-Ming Chiu, Chia-Ming Liang and Kua-Hua Lee, “Pulsewidth Control Loop with Dynamic Digitally Controlled Fast-Locking Schemes,” accepted by IET Circuits, Devices and Systems.
3. Hong-Yi Huang, Shin-Dian Jan, “All Digital Pulsewidth Control Loop,” revised by International Journal of Electronics.
4. Hong-Yi Huang, Yang Chou and Cheng-Yu Chen, “CMOS Differential Logic Circuits using Charge-Redistribution and Reduced-Swing Schemes,” IEICE Trans. Electronics, Feb. 2012.
5. Hong-Yi Huang, Chun-Chieh Wu, and Ching-Hsing Luo, “A Fractional-N PLL for MICS Band Application” Microelectronics, Journal, 2012.
6. Hong-Yi Huang and Bo-Ruei Wang “High-Gain High-Bandwidth Rail-to-Rail Constant-gm CMOS Operational Amplifier,” International Journal of Electronics, 2012.

7. Shih-Lun Chen, Hong-Yi Huang, and Ching-Hsing Luo, "Time Multiplexed VLSI Architecture for Real-Time Barrel Distortion Correction in Video-Endoscopic Images" IEEE Trans. Circuits and Systems for Video Technology, pp. 1612-1621, Nov. 2011.
8. Shih-Lun Chen, Hong-Yi Huang, and Ching-Hsing Luo, "A Low-Cost High–Quality Adaptive Scalar for Real-Time Multimedia Applications" IEEE Trans. Circuits and Systems for Video Technology, pp. 1600-1611, Nov. 2011.
9. Hong-Yi Huang and Ruei-Iun Pu "Differential Bidirectional Transceiver for On-chip Long Wires," Microelectronics Journal, vol. 42, no. 11, pp. 1208-1215, Nov. 2011.
10. Wei-Song Wang, Hong-Yi Huang, Shu-Chun Chen, Kuo-Chuan Ho, Chia-Yu Lin, Tse-Chuan Chou, Chih-Hsien Hu, Wen-Fong Wang, Cheng-Feng Wu, Ching-Hsing Luo, "Real-Time Telemetry System for Amperometric and Potentiometric", *Sensors, 11*, pp. 8593-8610, Sep., 2011.
11. Hong-Yi Huang and Jen-Chieh Liu, "All-Digital PLL Using Bulk-Controlled Varactor and Pulse-Based Digitally Controlled Oscillator," *Analog Integrated Circuits and Signal Processing*, vol. 68, no. 3, pp.245-255, Sep. 2011.
12. Kuo-Hsing Cheng, Jen-Chieh Liu, Hong-Yi Huang, Yu-Liang Li, and Yong-Jhen Jhu, "A 6 GHz Built-in Jitter Measurement Circuit Using Multi-phase Sampler" *IEEE Trans. on Circuits and Syst. II*, vol.19, no.58, pp.492-496, Aug. 2011.
13. Chiung-An Chen, Shih-Lun Chen, Hong-Yi Huang and Ching-Hsing Luo, "Asynchronous Multi-Sensor Micro Control Unit for Wireless Body Sensor Network (WBSN)", *Sensors, 11*, pp. 7022-7036, Jul., 2011.
14. Wei-Song Wang, Hong-Yi Huang, and Ching-Hsing Luo, "Wireless Biopotential Acquisition System for Portable Healthcare Monitoring" Journal of Medical Engineering & Technology, pp. 254-261, May, 2011.
15. Chia-Lin Chang, Chih-Wei Chang, Hong-Yi Huang, Chen-Ming Hsu, Chia-Hsuan Huang, Jin-Chern Chiou, and Ching-Hsing Luo, "A Power-Efficient Bio-Potential Acquisition Device with DS-MDE Sensors for Long-Term Healthcare Monitoring Applications", *Sensors* 10(5), pp. 4777-4793, May 2010.
16. Wei-Song Wang, Wei-Ting Kuo, Hong-Yi Huang and Ching-Hsing Luo, "Wide Dynamic Range CMOS Potentiostat for Amperometric Chemical Sensor", *Sensors* 10(3), pp.1782-1797, March 2010.
17. Shih-Lun Chen, Ho-Yin Lee, Chiung-An Chen, Hong-Yi Huang, and Ching-Hsing Luo, "Wireless Body Sensor Network With Adaptive Low-Power Design for Biometrics and Healthcare Applications," IEEE Systems Journal, vol. 3, no. 4, pp. 398 - 409, Dec. 2009.

18. Hong-Yi Huang and Shu-Feng Lee, "Digitally Programmable Rail-to-Rail CMOS Operational Amplifier as Reusable Silicon IP," Tamkang Journal of Science and Engineering, vol. 12, no. 4, pp. 409-415, 2009.
19. Shih-Lun Chen, Ho-Yin Lee, Chiung-An Chen, Hong-Yi Huang, and Ching-Hsing Luo, "An Architecture of Wireless Biomedical Sensor Network for Monitoring Applications", International J. of Electrical Eng., vol. 16, no.5, pp.403-409, Sep. 2009.
20. Hong-Yi Huang and Chia-Ming Liang, "Frequency Multiplier Using 50% Duty Cycle Corrector" IEICE Electronics Express Brief, Vol. 5, No. 22 pp.990-994, Nov. 2008.
21. Hong-Yi Huang and Shih-Lun Chen, "High-Speed Transition Detection Circuits for On-Chip Interconnects," Tamkang Journal of Science and Engineering, vol.9, no. 1, pp. 37-44, 2006.
22. Hong-Yi Huang and Jinn-Fu Lin, "Design and Application of CMOS Bulk Input Scheme," IEEE J. Solid-State Circuits, pp. 1305-1312, Aug. 2004.
23. Wei-Ming Lin and Hong-Yi Huang, "A Low-Jitter Mutual-Correlated Pulse Width Control Circuit," IEEE J. Solid-State Circuits, pp. 1366-1369, Aug. 2004.
24. Hong-Yi Huang and Shih-Lun Chen, "Interconnect Accelerating Techniques for sub-100nm Giga-Scale Systems," IEEE Trans. VLSI Systems, pp. 1192-1200, Nov. 2004.
25. 黃弘一，"IC 設計常見之十大問題" ，電子月刊， pp. 126-133. May, 2001,
26. Kuo-Hsing Cheng, Wei-Bin Yang, and Hong-Yi Huang, "The Charge Transfer Feedback-Controlled Split Path CMOS Buffer", *IEEE Trans. Circuits and Systems*, pp. 346-348, Mar. 1999.
27. 黃弘一、鄭國興、吳重雨,"局部非同步邏輯電路的真單相時脈架構,"*CCL Technical Journal* , pp. 63-70 , May. 1995
28. Hong-Yi Huang and Chung-Yu Wu, "New Design Methodology and New CMOS Differential Logic Circuits for the Implementation of Ternary Logic Systems in CMOS VLSI without Process Modification", *IEICE Trans. Electronics*, Vol. Vol.E77-C, No.6, p.960-969, Jun. 1994.
29. Chung-Yu Wu and Hong-Yi Huang, "Design and Application of Pipelined Dynamic CMOS Ternary Logic and Simple Ternary Differential Logic", *IEEE, J. Solid-State Circuits*, pp. 895-906, Aug. 1993.

Submitted Journal Papers

30. Hong-Yi Huang and Yen-Liang Lin "Mixed-Voltage I/O Buffer Using Blocked CMOS Transmission Gate," submitted to IET Circuits, Devices and Systems**.**
31. Hui-Wen Chang, Hong-Yi Huang, Yi-Hsiang Juan, Wei-Song Wang, Ching-Hsing Luo,"Adaptive Successive Approximation ADC for Biomedical Acquisition System" submitted to Microelectronics Journal.
32. Wei-Sheng Tseng, Hong-Yi Huang, Li-Wei Huang, and Kuo-Hsin Cheng, "A 0.18um 35mW 6-Gbit/s SATA Spread-Spectrum Clock Generator," submitted to IEEE Trans. Circuits and Systems, Part I.
33. Hong-Yi Huang, Chih-Yuan Hsu, Wei-Sheng Tseng, and Kuo-Hsin Cheng, "A 6-Gbit/s SATA Spread-Spectrum Clock Generator Using Onion Modulation," submitted to IEEE Trans. Circuits and Systems, Part I.
34. Hong-Yi Huang and Fu-Chien Tsai, "Design and Optimization of Arbitrary Stage Ring Oscillator Using Interpolating Scheme," submitted to IEEE Trans. Circuits and Systems, Part I.
35. Gilbert A.E. Matig-a, Hong-Yi Huang, Tim Chuang and Vincent Tien, "Programmable Analog Zero Equalization and Pre Emphasis Based LVDS Transceiver for MDDI PHY," submitted to IEEE Trans. Circuits and Systems, Part I.
36. Hong-Yi Huang, Shih-Chiang Hsu and Yi-Hsiang Juan, "High Sensitivity Low Voltage Temperature Sensor," submitted to Electronics Letter.
37. Kuo-Hsing Cheng, Jen-Chieh Liu, and Hong-Yi Huang, "An Ultra Low Voltage All-Digital PLL with a Digital Supply Regulator" submitted to IEEE JSSC.
38. Jen-Chieh Liu, Hong-Yi Huang, Kuo-Hsing Cheng and Yu-Tso Chen, "A 1.6~3.6-V 100-μA 8.38-MHz All-Digital PLL for Digital Water Meter," submitted to Microelectronics Journal.
39. Hong-Yi Huang, Ching-Chieh Wu and Rui-Iun Pu, "Design and Analysis of Simultaneously Bidirectional Transceivers," submitted to International Journal of Electronics.
40. Hong-Yi Huang and Ming-Da Lee, "Simultaneously Bidirectional Transceiver for High-Speed Inter-Chip Data Communications," submitted to IEICE Trans. Electronics.
41. Hong-Yi Huang and Ru-Jie Wang "Higher Order Temperature Terms Curvature-Compensated CMOS Bandgap Reference," submitted to IEICE Trans. Electronics**.**
42. Hong-Yi Huang and Ru-Jie Wang "Piecewise Linear Curvature-Compensated CMOS Bandgap Reference," submitted to IEICE Trans. Electronics**.**

劉萬榮教授

1. W. R. Liou, M. L. Yeh, and Y. L. Kuo, "A High Efficiency Dual-Mode Buck Converter IC For Portable Applications," *IEEE Trans. on Power Electronics*, Vol. 23, no. 2, pp. 667-677, March 2008 (SCI, Impact factor = 1.753, Rank 37/227)

2. W. R. Liou, M. L. Yeh , H. P. Hsich, and Y. J. Lin, " An EMI Reduced High-Efficiency Switching Power Amplifier," Recommended Publication in *IEEE Trans. on Power Electronics*, 2009 (SCI, Impact factor = 1.753, Rank 37/227)

3. W. R. Liou, T. H. Chen, M. L. Yeh, J. J. Ho, and G. E. Jan," A Low-Power 2/5.8GHz Dual-Wide-Band CMOS LC-VCO with Switched-Inductor Technique," *International Journal of Electronics*, Vol. 94, No. 6, pp. 623-632, June 2007. (SCI)

4. W. R. Liou, T. H. Chen, M. L. Yeh, and J. J. Ho, "A Low-Noise Low-Power 4.6-GHz CMOS VCO with Coupling Effect Reduced Inductors," *International Journal of Electronics*, Vol. 94, No. 2, pp. 107-121, February 2007. (SCI)

5. W. R. Liou, C.Y. Chen, J.J. Ho, C.K. Hsu, C.C. Chang, R. Y. Hsiao, and S. H. Chang " An improved alignment layer grown by oblique evaporation for liquid crystal devices," *Displays*, Vol. 27, No. 2, pp.69-72, 2006 (SCI)

6. M. L. Yeh, W. R. Liou, T. H. Chen, and Y. C. Lin, "A Low-Voltage Low-Power Programmable 5 GHz Frequency Synthesizer in Standard 0.18um CMOS Process," *International Journal of Electronics*, Vol. 93, No.2, pp.97-113, February 2006. (SCI)

7. J.J. Ho, C.Y. Chen, C.M. Huang, W. J. Lee, W.R. Liou, and C.C. Chang, " Ion-assisted sputtering desposition of antireflection film coating for flexible liquid-crystal display applications," *Applied Optics*, Vol. 44, No. 29, pp. 6176-6180, 2005 (SCI)

8. M. L. Yeh, W. R. Liou, T. H. Chen, and C. A. Tsai, "A Low-Voltage 4.6GHz Injection Locked Frequency Divider in Standard 1.8V 0.18um Complementary-Metal-Oxide-Silicon Technology", *Japanese Journal of Applied Physics*, Vol. 44, No. 1A, pp. 135-138, 2005 (SCI)

9. W.R. Liou, M.L. Yeh, C.A. Tsai, and S. H. Chang, " Design and implementation of a low-voltage 2.4-GHz CMOS RF receiver for wireless communication," *Journal of Marine Science and Technology*, Vol.13, No. 3, pp.170-175, September 2005. (SCI)

10. W. R. Liou, C. A. Tsai, M. L. Yeh, and G. E. Jan, 2004 "A 5.2GHz Low-Voltage Low-Noise Amplifier with 0.35um CMOS Technology", *International Journal of Electronics*, Vol. 91, No. 9, pp. 551-561, 2004 (SCI)

11. W.R. Liou, C. T. Kuo, M. L. Yeh, P. H. Chen, and Marynelle L. Z. Rosales, " A dual-mode step-up DC/DC converter IC with current-limiting and EMI reduction techniques, " Journal of Electronic Science and Technology of China, Vol. 6, No. 3, pp. 215-219, pp. 1332-1336, 2008 (Selected from the best paper award of 2008 IEEE International Conference on Communications, Circuits and Systems Proceedings)

12. W. R. Liou, C. A. Tsai, M. L. Yeh, and A. Y. Wu, "A Novel Current Control Pad for Electromagnetic Interference Solution", Japanese Journal of Applied Physics, Vol.43, No. 5A, pp.2462-2466 , 2004 (SCI)

13. C.A. Tsai, A.Y. Wu, W.R. Liou, and W.C. Lin, " Second Harmonic Generation in Barium Titanate Thin Films on Silicon Glass by Corona Poling," *Japanese Journal of Applied Physics,* Vol. 43, No. 4A, pp. 1348-1356, 2004 (SCI)

陳永源 教授

A. Journal Paper

1. Yung-Yuan Chen & Shambhu J. Upadhyaya, June 1993, "Reliability, Reconfiguration and Spare Allocation Issues in Binary Tree Architecture Based on Multiple-Level Redundancy," IEEE Trans. on Computers, VOL. 42, No.6, pp.713-723. (SCI)

2. Yung-Yuan Chen & Shambhu J. Upadhyaya, Sept. 1993, "Yield Analysis of Reconfigurable Array Processors Based on Multiple-Level Redundancy," IEEE Trans. on Computers, VOL. 42, No.9, pp.1136-1141. (SCI)

3. Yung-Yuan Chen & Shambhu J. Upadhyaya, June 1994, "Modeling the Reliability of a Class of Fault Tolerant VLSI/WSI Systems Based on Multiple-Level Redundancy," IEEE Trans. on Computers, VOL. 43, No.6, pp.737-748. (SCI)

4. Yung-Yuan Chen, Ching-Hwa Cheng and Yung-Ci Chou, Oct. 1994, "An Effective Reconfiguration Process for Fault-Tolerant VLSI/WSI Array Processors", First European Conference on Dependable Computing (EDCC-1), pp.421-438, Berlin, Germany. (Springer-Verlag: Lecture Notes in Computer Science 852) (SCI)

5. Gene Eu Jan, Ming-Bo Lin & Yung-Yuan Chen, June 1997, "Computerized Shortest Path Searching for Vessels," Journal of Marine Science and Technology, VOL.5, No.1, pp. 95-99.

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7. Yung-Yuan Chen, "Concurrent Detection of Processor Control Errors by Hybrid Signature Monitoring," Third European Dependable Computing Conference held in Prague, Czech Republic, pp. 437-454, September 1999. (Springer: Lecture Notes in Computer Science 1667) (SCI)

8. 陳永源，“利用看守狗處理器在同步偵錯上之研究”， 第四十二期國科會『工程科技通訊』， pp. 38-39, Dec. 1999。

9. Yung-Yuan Chen and Gene Eu Jan, “Resource Placement in Star Network,” Chung Hua Journal of Science and Engineering, Vol. 1, No. 2, pp.61-70, Sept. 2003.

10. Yung-Yuan Chen and Hung-Chuan Lai, “A Comprehensive Study of Fault-Tolerant VLIW Processors,” Chung Hua Journal of Science and Engineering, Vol. 2, No. 2, pp.49-54, June 2004.

11. Yung-Yuan Chen, “Embedding Watchdog Processor Scheme in VLIW Architecture,” Chung Hua Journal of Science and Engineering, Vol. 3, No. 1, pp. 153-159, Jan. 2005. (NSC 93-2213-E-216-019)

12. **Yung-Yuan Chen** and Kuen-Long Leu, “Signature-monitoring technique based on instruction-bit grouping,” *IEE Proceedings- Computers and Digital Techniques*, Vol. 152, No. 4, pp. 527-536, July 2005. (SCI, EI)

13. **Yung-Yuan Chen,** “Concurrent Detection of Control Flow Errors by Hybrid Signature Monitoring,” *IEEE Trans. on Computers*, Vol. 54, No. 10, pp. 1298-1313, October 2005. (SCI) (NSC 87-2213-E-216-001)

14. **Yung-Yuan Chen,** “Incorporating Fault-Tolerant Features in VLIW Processors”, *International Journal of Reliability, Quality and Safety Engineering*, Vol. 12, No. 5, pp. 397-411, October 2005. (EI) (NSC 89-2218-E-216-010 and NSC 90-2213-E-216-021)

15. **Yung-Yuan Chen**, “A Fault Diagnosis Scheme and Its Quality Issue in Reconfigurable Array Architecture,” *Journal of Computer Science and Technology*, Vol. 6, No. 1, pp. 12-21, April 2006.

16. **Yung-Yuan Chen,** Kuen-Long Leu and Chao-Sung Yeh, "Fault-Tolerant VLIW Processor Design and Error Coverage Analysis," *The 2006 IFIP International Conference on Embedded And Ubiquitous Computing*, pp. 754-765, August 2006. (Springer: Lecture Notes in Computer Science 4096) (SCI) (NSC 92-2213-E-216-005 and NSC 93-2213-E-216-019)

17. Yung-Yuan Chen, Kuen-Long Leu and Kun-Chun Chang, "Datapath Error Detection with Hybrid Detection Approach for High-Performance Microprocessors," *WSEAS Transactions on Computers*, Vol. 7, Issue 8, pp. 1337-1351, August 2008. (EI) (NSC 96-2221-E-216-006)

18. Yung-Yuan Chen, Chung-Hsien Hsu, and Kuen-Long Leu, "Analysis of System Bus Transaction Vulnerability based on FMEA Methodology in SystemC TLM Design Platform," *WSEAS Transactions on Computers*, Issue 2, Vol. 8, pp. 406-416, Feb. 2009. (EI) (NSC 97-2221-E-216-018)

19. Yung-Yuan Chen and Kuen-Long Leu, "Reliable Data Path Design of VLIW Processor Cores with Comprehensive Error-Coverage Assessment," *Microprocessors and Microsystems*, Vol. 34, Issue 1, pp. 49-61, Feb. 2010. (SCI) (NSC 96-2221-E-216-006 and NSC 97-2221-E-216-018)

20. Kuen-Long Leu, Yung-Yuan Chen, Chin-Long Wey, Jwu-E Chen and Chung-Hsien Hsu, "A Bayesian Network Reliability Modeling for FlexRay Systems," *World Academy of Science, Engineering and Technology*, Issue 41, pp. 42-47, May 2010. (EI) (NSC 98-2221-E-305-010 and 98-EC-17-A-02-S2-0017)

21. Yung-Yuan Chen and Gene Eu Jan, "Development of Scenario-Based Fault Injection Platform and Its Application Study," *Tamkang Journal of Science and Engineering*, Vol. 13, No. 2, pp. 205-214, June 2010. (EI)

22. Yung-Yuan Chen, "Development of SoC-level safety process in SystemC design platform for safety-critical systems," submitted to *Microprocessors and Microsystems* (full paper), August 2011. (SCI) (NSC 97-2221-E-216-018 and NSC 98-2221-E-305-010)

23. Yung-Yuan Chen, Shie-Lung Li, and Gene Eu Jan, "Development of Fault Scenario Generator Tool for FlexRay Communication Systems," Energy Procedia (ELSEVIER), Vol. 13, pp. 8938-8945, 2011. (EI) (NSC 99-2221-E-305-016)

24. Yung-Yuan Chen and Tong-Ying Juang, "Vulnerability Analysis and Risk Assessment for SoCs used in Safety-Critical Embedded Systems," a book chapter in "Embedded Systems – Theory and Design Methodology", ISBN 978-953-51-0167-3, edited by Kiyofumi Tanaka, published by InTech - Open Access publisher of books and journals in the fields of science, technology and medicine, pp. 51-72, March, 2012.

25. Yung-Yuan Chen, Che-Hao Chang and Gene Eu Jan, "Study the Effect of Delayed Frame Errors on FlexRay Communication Systems," *Advanced Science Letters*, Vol. 8, pp. 795-800, April 2012. (SCIE) (NSC 99-2221-E-305-016)

26. Kuen-Long Leu, Yung-Yuan Chen and Jwu-E Chen, "Hybrid of Bayesian Network and Markov Chain for FlexRay Systems Reliability Modeling," submitted to *IEEE Transactions on Vehicular Technology*, September 2012. (SCI) (NSC 100-2221-E-305-004 and NSC 101-2221-E-305-007)

27. Gene Eu Jan, Ming-Bo Lin, Cheng-Hong Li and Yung-Yuan Chen, "A Novel Design of Superconcentrator-Based Load Balancer for Highly Parallel Computers," to be published at *Advanced Science Letters*, August 2012. (SCIE)

28. Yung-Yuan Chen and Kuen-Long Leu, "Study the Effect of Soft Errors on FlexRay-Based Automotive Systems," *World Academy of Science, Engineering and Technology*, Issue 70, pp. 991-995, October 2012. (NSC 100-2221-E-305-004) (EI)

楊棧雲 教授

A. 期刊論文

1. Chan-Yun Yang, Jui-Jen Chou, Feng-Li Lian, Robust classifier learning with fuzzy class labels for large-margin support vector machines, *Neurocomputing*, To Appear, 2012. (SCI)
2. Chan-Yun Yang, Jr-Syu Yang, Feng-Li Lian, Safe and smooth: mobile agent trajectory smoothing by SVM, *International Journal of Innovative Computing Information and Contro*l, 8(7B): 4959–4978, 2012. (SCI)
3. Jian-Jun Wang, Chan-Yun Yang, Jia Jing, Estimation of approximating rate for neural network in L(ω,p) spaces, *Journal of Applied Mathematics*, 2012:Article ID 636078, 2012. (SCI)

4. Jianjun Wang, Bai-Li Chen, Chan-Yun Yang, Approximation of algebraic and trigonometric polynomials by feedforward neural networks, *Neural Computing and Applications*, 21(1): 73–80, 2012. (SCI)
5. Yao-Wen Hsueh, Chan-Yun Yang, Sensing tool breakage in face milling by support vector machine. *Advanced Materials Research*, 264-265:991-996, 2011. (EI)
6. Jianjun Wang, Chan-Yun Yang, Shukai Duan. Approximation order for multivariate Durrmeyer operators with Jacobi weights. *Abstract and Applied Analysis*, 2011:Article ID 970659, 2011. (SCI)
7. Chan-Yun Yang, Jr-Syu Yang, Jian-Jun Wang. Margin calibration in SVM class-imbalanced learning. *Neurocomputing*, 73:397–411, 2009. (SCI)
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