國立臺北大學電機工程研究所學生發表會議/期刊論文紀錄

學生姓名	指導教授	論文題目	會議/期刊名稱	會議時間地點/期刊出刊資訊	備註
郭仰倫	陳永源教授	An Autonomous Recovery Software Module for Protecting Embedded OS and Application Software	2012 IEEE Global High Tech Congress on Electronics	18-20 Nov. 2012/ China, Shenzhen	
劉家銘	陳永源教授	ECU-Level Fault-Tolerant Framework for Safety-Critical FlexRay Network Systems	International Conference on ICT Convergence 2012	15-17 Oct. 2012/ Korea, Jeju	
劉家銘 張哲豪	陳永源教授	FlexRay 通訊系統的容錯技術探討	2012 SAE International Conference	9 Nov.2012/ Taiwan	
李霈穎	黃弘一副教授	A Fractional-N PLL for MICS Band Application	The 22nd VLSI Design/CAD Symposium	雲林劍湖山王子大飯店 2011 年 08 月 02 日至 05 日	
陳琨元	黃弘一副教授	Simultaneously Bidirectional Transceiver for High-Speed Inter-Chip Data Communications	The 22nd VLSI Design/CAD Symposium	雲林劍湖山王子大飯店 2011 年 08 月 02 日至 05 日	
葉庭嘉	黃弘一副教授	External Capacitorless Low Dropout Linear Regulator using Cascode Structure	The 23nd VLSI Design/CAD Symposium	屏東墾丁福華渡假飯店 2012 年 8 月 7 日至 8 月 10 日	
謝秉哲	黃弘一副教授	Design and Optimization of Arbitrary Stage Ring Oscillator Using the Interpolating Scheme	The 23nd VLSI Design/CAD Symposium	屏東墾丁福華渡假飯店 2012 年 8 月 7 日至 8 月 10 日	
嚴紹祖	黃弘一副教授	Near-Field Wireless Power Integrated Circuit Without	The 23nd VLSI Design/CAD Symposium	屏東墾丁福華渡假飯店 2012 年 8 月 7 日至 8 月 10	

		External Capacitors		日	
陸奕成 王世賢 陳偉智	劉萬榮 教授	Integrated Multi-Channel High Accuracy Current Control LED Driver With Low Dropout Regulator		2012/Doshisha University	
Yu-Ting Kuo	詹景裕 教授	A New Constant Time Analog Rank Order Filter with O(n) Complexity	*The 3rd International Conference on Advanced Computer Theory and Engineering*, V6-23 - V6-26	Chengdu, China TIBET HOTEL CHENGDU, 20-22 August, 2010	
陳銘恩	詹景裕 教授	Analysis of Just-In-Time Inventory System	中華民國工業工程學會 99 年學術論文研討會，Southern Tainan Univ., Tainan, Taiwan, B7-1		
黃郁書	詹景裕 教授	The Most Economical Route Planning on the Smartphone	中華民國運輸學會 99 年學術論文國際研討會，Fon Chia Univ., Taichung, Taiwan, pp. 1169~1182	2010 年 12 月 9 日(星期四) 至 10 日(星期五), 逢甲大學人言大樓	
林志餘	詹景裕 教授	An Automatic Seat Assignment System	*Proceedings of Automation* 2010, Chung Yuan Univ., Chung-Li, Taiwan, pp. 850~856	Chung Yuan Univ., Chung-Li, Taiwan	
陳泰均	詹景裕 教授	An Optimal Channel Assignment Algorithm	*Proceedings of Automation* 2010, Chung Yuan Univ., Chung- Li, Taiwan, pp. 1032~1035	Chung Yuan Univ., Chung-Li, Taiwan	
Ted Chen	詹景裕 教授	A Fast Channel Assignment Algorithm	2011 *International Conference on Computer Science and Logistics*	11th to 13th November 2011 Zhengzhou, Henan, China	

			Engineering, Zhengzhou, China, pp. 175-179		
Yu-Shu Huang	詹景裕教授	Practical Route Planning on the Smart Phones	*WASET International Conference on Computational Mathematics* (ICCM2011), Paris, France, pp. 1-6	December 21, 2011-December 23, 2011	
J. J. Hsu	詹景裕教授	A Fastest Rectilinear Steiner Tree Algorithm Based on the H-tree	*Proceedings of National Computer Symposium*, Vol. 3: *Computer Architectures, Embedded System and VLSI/EDA*, Taiwan, pp. 20-27	中華民國 100 年 12 月 2-3 日，國立嘉義大學	
H. W. Chen	詹景裕教授	A Fast Maze Routing Approach to the Steiner Tree Problem	*Proceedings of National Computer Symposium*, Vol. 3: *Computer Architectures, Embedded System and VLSI/EDA*, pp. 180-188	中華民國 100 年 12 月 2-3 日，國立嘉義大學	
Y. C. Wu	詹景裕教授	Practical Route Planning on the Smartphones	*The 2011 International Conference and Annual Meeting of Chinese Inst. of Transportation*, Chiao Tung Univ. Hsinchu, Taiwan, pp. 1152-1171	1-2 December, 2011, National Chiao Tung University	
黃耀正	詹景裕教授	實作網路攝影機之自動對焦與變焦追蹤	智慧型數位生活研討會, Chinese Culture Univ., Taipei, Taiwan, pp. 529-535	2011 年 4 月 29 日，中國文化大學	

Wei Chun Tsai	詹景裕教授	A Delaunay triangulation- based shortest path algorithm with O(n log n) time in the Euclidean plane	2012 *IEEE/ASME International Conference on Advanced Intelligent Mechatronics*, pp. 186-189	July 11-14, 2012, KaoHsiung, Taiwan	
Y.-H. Liu	詹景裕教授	An improved approach among the Delaunay triangulation-based Steiner minimal tree algorithms with obstacle- avoidance	*Electronic Technology Symposium*, EO-10209174	中華民國 101 年 6 月 1 日 義守大學	最佳論文佳作獎
翁嘉偉	何善輝教授	A Continuous Optimized Data Dependence Testing For Reducin The Complexity Of Source Level Debugging For Parallel Compiler And Vector Compiler Optimizations	**2011** 第十二屆科學與管理學術研討會	10/27/2011 國立台北科技大學<科技大樓 B2 國際會議廳>	
詹宇翔	何善輝教授	A Non-Continuous Optimized Data Dependence Testing For Reducing The Complexity Of Source Level Debugging For Parallel Compiler And Vector Compiler Optimizations	**2011** 第十二屆科學與管理學術研討會	10/27/2011 國立台北科技大學<科技大樓 B2 國際會議廳>	
詹宇翔	何善輝教授	DNA Sequence Assembly with Bioinformatics Shotgun Method	2012 International Conference on Biomedical Engineering and Biotechnology	05/30/2012 University of Macau	
陳翔靖	何善輝教授	Constructing the Chor-Rivest Knapsack Cryptosystem on a DNA-based Computer	2011 第六屆積體光機電科技與智慧財產權實務研討會	12/20/2011 台灣大學電機工程學系博理館 101 演講廳	

林育正	何善輝 教授	Constructing Bio-logic and Bio-Arithmetic Circuitry of Parallel Adder, Subtractor, Multiplier, Divider and Modular in the Adleman-Lipton Model	2011 第六屆積體光機電科技與智慧財產權實務研討會	12/20/2011 台灣大學電機工程學系博理館 101 演講廳	

會議發表記錄

姓名	劉家銘	學號	710082302
會議名稱	International Conference on ICT Convergence 2012		
會議日期	15-17 Oct. 2012	會議地點	Korea, Jeju
論文作者	陳永源、劉家銘		
論文題目	ECU-Level Fault-Tolerant Framework for Safety-Critical FlexRay Network Systems		
論文摘要: FlexRay, as a communication protocol for automotive control systems, is developed to fulfill the increasing demand on the electronic control units for implementing systems with higher safety and more comfort. In this paper, we propose an effective ECU-level fault-tolerant framework for safety-critical FlexRay network systems. The proposed framework employs the global redundancy scheme with the task migration to sustain the operation of system when the failure of ECUs occurs. Two types of task migration scheme are presented. One is the FlexRay cluster has no capability of task migration among backup (or called redundant) nodes and the other is contrary to that. We develop the reliability model for the analysis of our fault-tolerant FlexRay systems. The reliability analysis with various numbers of backup nodes, system sizes and ECU failure rates are conducted and the reliability results are provided and discussed.			

會議發表記錄

姓名	劉家銘	學號	710082302
會議名稱	2012 SAE International Conference		
會議日期	9 Nov. 2012	會議地點	Taiwan
論文作者	陳永源、劉家銘、張哲豪		
論文題目	FlexRay 通訊系統的容錯技術探討		
論文摘要: 隨著高安全度車用電子線傳控制系統應用的來臨，可靠度與安全性議題變成一項相當重要的課題，錯誤注入與容錯機制在可靠度與安全性上扮演了一相當重要的角色。本研究依據EN50159所規範的錯誤類型，提出FlexRay錯誤注入			

平台。利用錯誤情境產生器產生錯誤情境測試檔案，將所設定的錯誤情境執行於通訊匯流排上正在傳輸的訊框(Frame)，加速系統的失敗，並用TTX Connexion來蒐集通訊匯流排上的資料。本論文以個案研究的方式，開發簡易的FlexRay線傳轉向(steer-by-wire)控制系統，搭配錯誤注入平台，探討通訊匯流排上的訊框發生錯誤，對系統的影響，以及驗證FlexRay通訊協議所提供的容錯機制的有效性。我們在實驗中針對不同action point offset (APO)與static slot參數的設定，以及使用不同個數的同步節點設置，來測試系統在不同長度的訊框延遲錯誤情況下，對於訊框接收成功率以及時脈同步容錯的有效性與優劣性，並分析系統發生Missing_Term時之失敗行為。

會議發表記錄

姓名	李霈穎	學號	79982106
會議名稱	The 23nd VLSI Design/CAD Symposium		
會議日期	2011 年 08 月 02 日至 05 日	會議地點	雲林劍湖山王子大飯店
論文作者	Hong-Yi Huang and Pei-Ying Lee		
論文題目	A Fractional-N PLL for MICS Band Application		
論文摘要: This presents a fractional-N phase-locked loop (PLL) circuit being implemented with active inductors and auto-calibration technology. In this work, the active inductors and the capacitors of the loop filter were implemented with MOSFET for decreasing the area of chip greatly. This PLL circuit achieves smaller chip area and provides a wider range of the output frequency. Moreover, the proposed auto-calibration technique would reduces and overcome the effect of the voltage, temperature and process variations. The measurement results have shown that the proposed Fractional-N PLL chip, with a die size of 450 385 um2, chieves phase noise @ 1MHz of -105.5dBc/Hz, operating frequency range from 218 MHz to 466 MHz, and power consumption of 5.13 mW at 402MHz (excluding output buffer). This chip was fabricated using TSMC 0.18 μm 1P6M CMOS process technology.			

姓名	陳琨元	學號	79982104
會議名稱	The 23nd VLSI Design/CAD Symposium		
會議日期	2011 年 08 月 02 日至 05 日	會議地點	雲林劍湖山王子大飯店
論文作者	Ming-Ta Lee and Kun-Yuan Chen		
論文題目	Simultaneously Bidirectional Transceiver for High-Speed Inter-Chip Data Communications		
論文摘要: A CMOS low dropout regulator (LDR) with high power supply rejection (PSR) and an on-chip output capacitor is proposed for biomedical implantable			

integrated circuit. To achieve a high PSR over a wide frequency range, a cascade technique with power NMOS and with power PMOS is utilized. A cascode technique is used to increase the output impedance of the LDR so that the output voltage can be less susceptible to any changes in the input voltage. With this technique, a clean and stable voltage can be produced. The test chip is implemented by TSMC 0.18um 1P6M process. The chip area is 0.872×0.561 mm2, the measured PSR at full load without using large external output capacitor is -37.7 dB at 60MHz and the ripple is 7.76mV, the power consumption is 2.13 mW and the efficiency is 77%. Index Terms—Current Feedback Compensation, Capacitor-Free LDO, Power Supply Rejection (PSR).

姓名	葉庭嘉	學號	710082109
會議名稱			
會議日期	2012 年 8 月 7 日至 8 月 10 日	會議地點	屏東墾丁福華渡假飯店
論文作者	Cheng-Yu Chen and Ting-Chia Yeh		
論文題目	External Capacitorless Low Dropout Linear Regulator using Cascode Structure		

論文摘要: A CMOS low dropout regulator (LDR) with high power supply rejection (PSR) and an on-chip output capacitor is proposed for biomedical implantable integrated circuit. To achieve a high PSR over a wide frequency range, a cascade technique with power NMOS and with power PMOS is utilized. A cascode technique is used to increase the output impedance of the LDR so that the output voltage can be less susceptible to any changes in the input voltage. With this technique, a clean and stable voltage can be produced. The test chip is implemented by TSMC 0.18um 1P6M process. The chip area is 0.872×0.561 mm2, the measured PSR at full load without using large external output capacitor is -37.7 dB at 60MHz and the ripple is 7.76mV, the power consumption is 2.13 mW and the efficiency is 77%. Index Terms—Current Feedback Compensation, Capacitor-Free LDO, Power Supply Rejection (PSR).

姓名	謝秉哲	學號	710082107
會議名稱			
會議日期	2012 年 8 月 7 日至 8 月 10 日	會議地點	屏東墾丁福華渡假飯店
論文作者	Design and Optimization of Arbitrary Stage Ring Oscillator Using the Interpolating Scheme		
論文題目	External Capacitorless Low Dropout Linear Regulator using Cascode Structure		

論文摘要: This work proposes a multi-phase voltage controlled oscillator (VCO) using the interpolating scheme. The N-stage ring oscillator with k-stage

sub-feedback loops (where N is not a multiple of k) has N output phases and operational frequency as high as k-stage sub-feedback loops. The circuit analysis and simulated verification are also described for an optimized design. The first order linear inverter model of the proposed ring oscillator defines the relationship between operational frequency and phase numbers. In the proposed topology, the operational frequency is not decreasing while the stage number of ring oscillator is increasing. This multi-phase VCO is verified in a 5-GHz and 12-phase phase-locked loop. The test chip is implemented in a 0.18 μm CMOS process and the core area is 260 × 355 μm2. The power consumption is 127 mW with I/O buffers. The RMS jitter and peak-to-peak jitter are 1.46 ps and 10.5 ps, respectively.

姓名	嚴紹祖	學號	710082110
會議名稱			
會議日期	2011 年 08 月 02 日至 05 日	會議地點	雲林劍湖山王子大飯店
論文作者	Ding-Yu Wei and Shao-Zu Yen		
論文題目	Near-Field Wireless Power Integrated Circuit Without External Capacitors		

論文摘要: A near-field wireless power integrated circuit without external capacitors is proposed in this paper. The only external component is the coupling coil. The verstress problem in a low voltage process is eliminated which improves the reliability. The test chip is implemented using a 0.18μm CMOS process with a core area of 0.804 × 0.786 mm2. The carrier frequency for wireless power transmission is 13.56MHz. The measurement result shows that the receiver can generate a stable 1.8V DC output voltage to supply 1mA output current under different amplitudes of the coupling input voltage from the transmitter. The output voltage ripple is 14mV.

會議發表記錄

姓名	翁嘉偉	學號	710082303
會議名稱	**2011** 第十二屆科學與管理學術研討會		
會議日期	10/27/2011	會議地點	國立台北科技大學
論文作者	Michael Shan-Hui Ho, David Chia-Wei Wong, Matt Yu-Shiang Gen		
論文題目	A Continuous Optimized Data Dependence Testing For Reducin The Complexity Of Source Level Debugging For Parallel Compiler And Vector Compiler Optimizations		

論文摘要:

Shen et al. indicate that one, two, and three-dimensional array references approximately account for, respectively, 56, 36 and 8 percent of the examined array references. Jaramillo also points out that loop normalization makes array references

more complex and creates many difficulties of source level debugging for parallel compilers and vector compilers. The modified I optimization test, a refined combination of the GCD and Banerjee tests, presents an efficient and optimized data dependence test technique to determine whether integer-valued solutions exist for one-dimensional arrays with constant bounds and *one-increment*.

姓名	詹宇翔	學號	710082301
會議名稱	**2011** 第十二屆科學與管理學術研討會		
會議日期	10/27/2011	會議地點	國立台北科技大學
論文作者	Michael Shan-Hui Ho, Matt Yu-Shiang Gen, David Chia-Wei Wong		
論文題目	A Non-Continuous Optimized Data Dependence Testing For Reducing The Complexity Of Source Level Debugging For Parallel Compiler And Vector Compiler Optimizations		

論文摘要:

Shen et al. indicate that one, two and three-dimensional array references approximately account for, respectively, 56, 36 and 8 percent of the examined array references. Jaramillo also points out that loop normalization makes array references more complex and creates many difficulties of source level debugging for parallel compilers and vector compilers. In this paper, we propose the non-continuous I optimization test to determine whether there are integer-valued solutions for one-dimensional arrays with constant bounds and non-one-increment. Experiments with benchmarks, cited from Livermore and Vector Loop, reveal that there are definitive results for most of one-dimensional arrays tested.

姓名	詹宇翔	學號	710082301
會議名稱	2012 International Conference on Biomedical Engineering and Biotechnology		
會議日期	05/30/2012	會議地點	University of Macau
論文作者	Michael Shan-Hui Ho, Kun-Yu Hung , Chaochang Chiu , Matt Yu-Shiang Gen		
論文題目	DNA Sequence Assembly with Bioinformatics Shotgun Method		

論文摘要:

DNA sequence assembly is a set of genomic sequences that can be assembled, condensed and oriented in order by applying the sequence homology along with mapping information to create a consensus sequence of a chromosome. The DNA sequence assembly problem has been recognized as NP-hard. In this paper, a newly developed DNA sequence assembly approach along with the bioinformatics shotgun

and Hamiltonian path finding methods is introduced and required for exact matches of any DNA sequence to solve worldly well-known DNA sequence assembly problem in polynomial time $O(n^6)$.

姓名	陳翔靖	學號	79982309
會議名稱	2011 第六屆積體光機電科技與智慧財產權實務研討會		
會議日期	12/20/2011	會議地點	國立台灣大學
論文作者	Michael Shan-Hui Ho, Shiang-Jing Chen, Yu-Shiang Gen and Yu-Cheng Lin		
論文題目	Constructing the Chor-Rivest Knapsack Cryptosystem on a DNA-based Computer		

論文摘要:

In recent years, research into bioinformatics computing greatly impacted practical public-key cryptosystems constructed on the bases of integer factoring [1] such as RSA. The Knapsack-Type Public Key Cryptosystem[3] is one of the viable public-key cryptosystem. Knapsack cryptosystems have the advantages of encryption and decryption speed[2] compared to other public-key cryptosystems. In this paper we use bio-logic arithmetic computing to constructing the Chor-Rivest Knapsack cryptosystem on a DNA-based computer.

姓名	林育正	學號	79982308
會議名稱	2011 第六屆積體光機電科技與智慧財產權實務研討會		
會議日期	12/20/2011	會議地點	國立台灣大學
論文作者	Michael Shan-Hui Ho, Yu-Cheng Lin, Yu-Shiang Gen and Shiang-Jing Chen		
論文題目	Constructing Bio-logic and Bio-Arithmetic Circuitry of Parallel Adder, Subtractor, Multiplier, Divider and Modular in the Adleman-Lipton Model		

論文摘要:

The advantages of bioinformatics computing have attracted many researchers to solve many NP problems in recent years. As Adleman proposed before, the DNA strands employed towards calculating solution to the NP-complete hamiltonian path problem (HPP). Lipton also demonstrated that adleman's techniques could be used to solve the satisfiability (SAT) problem. Based upon DNA massive parallelism features and DNA special manipulations in utilizing the logic circuitry gates, we developed basic bio-logical parallel AND, OR, and XOR gates which are used to construct bio-logic arithmetic units for NP problem solving in the Adleman-Liption model. They are Bio-arithmetic parallel adder, subtractor, multiplier, divider and modular.